



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

08/890,894 07/10/97 CHAUVEL

G TIF-15767A

023494 TM02/0515
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS TX 75265

EXAMINER

TRAN, D

ART UNIT

PAPER NUMBER

2186

DATE MAILED:

05/15/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

08/890,894

Applicant(s)

CHAUVEL ET AL.

Examiner

Denise Tran

Art Unit

2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 February 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6-15, 17, 19 and 34-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6-15, 17, 19 and 34-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____

Art Unit: 2186

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.
2. Claims 1-5, 16, 18, and 20-33 have been canceled. Claims 6-15, 17, 19, and 34-39 are presented for examination.
3. The following guidelines illustrate the preferred layout and content for patent applications. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

The following order or arrangement is preferred in framing the specification and, except for the reference to "Microfiche Appendix" and the drawings, each of the lettered items should appear in upper case, without underlining or bold type, as section headings. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) Title of the Invention.
- (b) Cross-References to Related Applications.
- © Statement Regarding Federally Sponsored Research or Development.
- (d) Reference to a "Microfiche Appendix" (see 37 CFR 1.96).
- (e) Background of the Invention.
 1. Field of the Invention.
 2. Description of the Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (f) Brief Summary of the Invention.
- (g) Brief Description of the Several Views of the Drawing(s).
- (h) Detailed Description of the Invention.
- (I) Claim or Claims (commencing on a separate sheet).
- (j) Abstract of the Disclosure (commencing on a separate sheet).
- (k) Drawings.
- (l) Sequence Listing (see 37 CFR 1.821-1.825).

Art Unit: 2186

4. The specification should have section headings.
5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 6-15, 17, 19, and 34-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17, recites the limitation "only one of said first" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites the limitation "said protocol processor" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim.

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "core" in claims 6 and 36-39 is used by the claims to mean

Art Unit: 2186

"processor," while the accepted meaning is "one of the types memory built into computers before RAM or main memory."

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 6-7, 9, 10-15, 17 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (hereinafter Aoyama) in view of Asano et al., U.S. Patent No. 5237686, (hereinafter Asano).

As per claims 6 and 36, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601); a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory circuit for coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8,

Art Unit: 2186

lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

As per claims 7, Aoyama shows the use of the second processor being a main processor (e.g., col.4, line 63 and et seq.).

As per claim 9, Aoyama does not specifically show the second processor as a DSP. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system

Art Unit: 2186

of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality.

As per claims 10-13, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM. Asano (e.g., figs. 1-2, els 22, 17; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of having a local memory as RAM and a program memory for each processor are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the system of Aoyama because it would allow a storage location to be read and written in any order by having local RAM and increase processing speed of each processor by having local RAM memories and program memories, thereby increasing the processing efficiency for each processor. Aoyama and Asano does not explicitly show a program memory as a ROM. "Official Notice" is taken that both the concept and advantages of providing; a program memory as ROM are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include ROMs into the system of Aoyama because it would allow a storage system not to loose data when power is removed from it.

As per claim 14, 15, and 17, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig.1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g.,

Art Unit: 2186

cols. 5-6). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

10. Claims 8 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Morris Mano, Computer System architecture, 1982, pages 264 and 282-283, (hereinafter Mano).

As per claim 8, Aoyama does not specifically show the scalar processor as a microprocessor. Mano, page 264, line 8 and et seq., is cited merely as an example to show both

Art Unit: 2186

the concept and advantages of providing a processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a processor into a microprocessor to Aoyama because it would provide for a reduction in space and signal lines between functional elements, leading to an increase in processing performance, and a low cost.

As per claim 35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of vector processing including signal processing tasks generally carrying out by a DSP and matrix computation performed by an array processor. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase system functionality. Mano, e.g., page 282 line 36 and et seq., has been cited as an example to show that both the concept and advantages of providing vector processing including the use of array processor for performing matrix computations are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include an array processor performing array computations into

Art Unit: 2186

Aoyama because it would allow parallel computations on large arrays to be performed, thereby, increasing system computation power.

11. Claims 19, 34-35 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of applicant's admitted prior art, Background of the invention, the instant specification page 1 line 6 to page 2, line 11, (hereinafter AAPA).

As per claims 34-35, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. Asano (e.g., col. 1, line 9 and et seq.) has been cited as merely one example, to show the concept and advantages of providing DSP to perform signal processing are well known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to apply the teaching of Asano into the vector processing system of Aoyama because it would provide signal processing capability to suit a special purpose application, thereby increase

Art Unit: 2186

system functionality. Also, AAPA, the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing or a protocol processor; and vector processing including the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing and an array processor performing array computations into Aoyama because it would allow protocol processing to be performed and parallel computations on large arrays to be performed, thereby, increasing system computation power and functionality.

As per claim 19, Aoyama shows the use of providing an instruction set to the first scalar processor, comprising at least one field of execution conditions and classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers (i.e., scalar operations) (e.g., col.3, line 20 and et seq.); transfer operations between the memory and a register in the scalar processor; and monitoring for all of the operations modifying a value of an incrementation register inherently (i.e., a value of $I=1$ to N in Do loop being increased by an inherently incrementation register or a counter) (e.g. col.1, line 41 and et seq.). Aoyama does not explicitly shows a transfer operations between a protocol processor and memory. AAPA, the instant specification, e.g., page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing a processor to perform protocol processing are

Art Unit: 2186

well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed thereby, increasing system functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601) where the first processor being suited to execute tasks to which a main processor is not suited; a second processor or the main processor (e.g., col.4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well

Art Unit: 2186

known and expected in the computer art. It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. AAPA, the instant specification page 1 line 6 to page 2, line 11, has been cited as an example to show that both the concept and advantages of providing protocol processor for performing protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing because it would allow protocol processing to be performed; thereby, increasing system functionality.

12. Claims 19, 34 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4964035, (herein after Aoyama) in view of Asano et al., U.S. Patent No. 5237686 (hereinafter Asano), further in view of Finch et al., U.S. Patent No. 4783778, (hereinafter Finch).

As per claim 34, Aoyama teaches the vector processor and matrix computations (e.g., fig. 1., els 500 and 600 and cols. 2, line 5 and et seq.) ; and the scalar processor (e.g., fig. 1., els 500

Art Unit: 2186

and 600 and cols.2, line 5 and et seq.) but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing. Finch, e.g., col. 8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing or protocol processor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

As per claim 19, Aoyama shows the use of providing an instruction set to the first scalar processor, comprising at least one field of execution conditions and classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers (i.e., scalar operations) (e.g., col.3, line 20 and et seq.); transfer operations between the memory and a register in the scalar processor; and monitoring for all of the operations modifying a value of an incrementation register inherently (i.e., a value of $I=1$ to N in Do loop being increased by an inherently incrementation register or counter) (e.g. col. line 41 and et seq.). Aoyama does not explicitly shows a transfer operations between a protocol processor and memory. Finch, e.g., col. 8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol

Art Unit: 2186

processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

As per claims 37-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig.1, el. 600), comprising a core (e.g., fig.1, el. 601) where the first processor being suited to execute tasks to which a main processor is not suited; a second processor or the main processor (e.g., col.4, line 63 and et seq.), for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core (e.g., fig. 1, els. 501); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig.1, els 810 or 800a, cols. 5-6); and a common memory coupling the first processor to the second processor (e.g., fig.1, el. 800). Even though Aoyama teaches the use of a local buffer, and a program register of a scalar processor (e.g., fig.1, els. 601 and 602; and col. 5, lines 47 et seq.); and a local register and program register of a vector processor (e.g., fig. 1, el. 502; and col. 8, lines 4 et seq.). Aoyama does not explicitly show the use each of the processors comprising a local memory and a program memory and one and only one common memory (the main storage 1 or 700 as a common memory) coupling the local memory of the first processor to the local memory of the second processor. Asano (e.g., fig. 1, 6, el. 62; and col. 9, line 56 and et seq.) has been cited as merely one example, teaching the concept and advantages of each processor having a local memory and a program memory and a common memory for coupling the local memory of a first processor to the local memory of a second memory are well known and expected in the computer art. It would have been obvious to one of ordinary skill in

Art Unit: 2186

the computer art at the time the invention was made to have a local memory and a program memory and one and only one common memory for coupling the local memory of a first processor to the local memory of a second memory into the system of Aoyama because it would increase processing speed of each processor by having local memories and program memories instead of a main storage, thereby increasing the processing efficiency for each processor.

Aoyama and Asano do not explicitly show the use of the first processor being a protocol processor. Finch, e.g., col.8, line 42 and et seq., has been cited as an example to show that both the concept and advantages of providing a protocol processor performs protocol processing are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor performing protocol processing into Aoyama because it would allow protocol processing to be performed, thereby, increasing system computation functionality.

13. Applicant's arguments filed 2/5/01 have been fully considered but they are not persuasive.

14. In the remarks, the applicant argued (1) that Aoyama fig. 1 shows it is control logic 810 coupled the first and second processors not common memory 800.

In response to the applicant's argument (1), in fig.1, Aoyama also shows the control logic 810 coupled to the common memory 800.

Art Unit: 2186

15. In the remarks, the applicant's argued (2) that Aoyama discloses RAMs 108 not a DPRAM.

In response to the applicant's argument (2), in fig.5, Aoyama discloses the common RAM 108 memory has dual ports.

16. In the remarks, the applicant argued (3) that the examiner's obviousness rational is improper hindsight reconstruction.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

17. Applicant's arguments with respect to other arguments regarding to claims 6-15, 17, 19 and 34-39 have been considered but are moot in view of the new ground(s) of rejection.

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2186

- A) Swoboda et al. (60853360) is cited to show a multiprocessor system including: DSPs, a microprocessor, and an array processor.
- B) Zurawski et al. (5210834) is cited to show a scalar and vector processors.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday and Thursday from 8.30 to 6.00 p.m..


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.



Denise Tran

01/06/00



MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 21st